ABSTRACT

A serial-to-parallel/parallel-to-serial conversion engine provides a bi-directional interface between a serial TDM highway and a parallel TDM highway. The conversion engine includes a serial-to-parallel data conversion device receives a serially received data word and provides a parallel output data word. The conversion engine includes a serial data input interface that receives the serially received data word and provides a received data word. A serial-to-parallel mapping circuit receives the received data word and generates memory write control and write address signals. A memory device includes a first port responsive to the memory write control signals and write address signals for writing the received data word into the memory device, and a second port responsive to memory read control and read address signals for reading data from the memory device. Output interface circuitry generates the memory read control and read address signals, and receives output data from the memory device and reorders the bits of the parallel output data to provide the parallel data word. The conversion engine also includes a parallel-to-serial conversion device that receives a parallel received data word and provides a serial data word. The parallel-to-serial conversion device includes a memory device having a first port responsive to memory write control and write address signals, and a second port responsive to memory read control and read address signals. A parallel-to-serial mapping circuit receives the parallel received data word and generates the memory write control and write address signals to write a bit shuffled version of the parallel received data word into the memory device. A data output interface generates the memory read control and read address signals to perform reads from the memory device and receives output data from the memory device to provide the serial data word.